IN THE CLAIMS:

Claim 1 (withdrawn): A semiconductor device comprising:

a semiconductor substrate including an element partitioning trench and a mask aligning trench;

a first insulation deposited in the element partitioning trench; and

a second insulation partially deposited in the mask aligning trench formed from the same substance as the first insulation.

Claim 2 (withdrawn): The semiconductor device according to claim 1, wherein the mask aligning trench has a upper edge, and wherein an upper surface of the second insulation defines a step with the upper edge.

Claim 3 (currently amended): A method for manufacturing a semiconductor device, the method comprising:

forming an element partitioning trench and a mask aligning trench in a semiconductor substrate;

simultaneously depositing an insulation in the element partitioning trench and the mask aligning trench by a chemical vapor deposition process consisting of high density plasma chemical vapor deposition, wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

applying a protective mask on the insulation deposited in the element

partitioning trench;

etching the insulation deposited in the mask aligning trench to remove some of the insulation; and

flattening an upper surface of the semiconductor substrate.

Claim 4 (Original): The method according to claim 3, wherein the step of forming the element partitioning trench and the mask aligning trench includes:

forming a coating on the semiconductor substrate,

wherein the coating has a pattern of openings corresponding to the element partitioning trench and the mark aligning trench; and

etching the semiconductor substrate using the coating as a mask to form the element partitioning trench and the mask aligning trench, wherein the insulation depositing step includes depositing the insulation without removing the coating.

Claim 5 (Original): The method according to claim 4, wherein the flattening step is performed through rotary grinding, and the coating functions as a stopper.

Claim 6 (Original): The method according to claim 5, wherein the semiconductor substrate is a silicon substrate, the insulation is formed from silicon oxide, and the coating is formed from silicon nitride, the method further comprising the step of forming a silicon oxide film on the semiconductor substrate prior to the formation of the element partitioning

trench and mask aligning trench, wherein the coating is formed on the silicon oxide film.

Claim 7 (Currently Amended): A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a silicon oxide film on an upper surface of a semiconductor substrate;

forming a silicon nitride film on the silicon oxide film;

partially removing the silicon nitride film and the silicon oxide film;

forming an element partitioning trench and a mask aligning trench by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths;

simultaneously depositing a first layer of insulation and a second layer of insulation in the element partitioning trench and in the mask aligning trench, respectively by a chemical vapor deposition process consisting of high density plasma chemical vapor deposition, wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

coating the first insulation with a protective mask;

etching the second insulation so that a step is formed between an upper surface of the semiconductor substrate and an upper surface of the second insulation; and

removing the protective mask.

Claim 8 (Original): The method according to claim 7, wherein the first insulation and the second insulation are made of the same material.